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#17	(metastable<in>metadata) and simulation and synthesis
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Simulation and synthesis AND (metastable and flip ANI [Search]

☑ Journal sources ☑ Preferred Web sources ☑ Other Web sources ☐ Exact phrase

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1. CummingsMills_Resets_final5.PDF [PDF-65K]
Apr 2003
...leading edge, the **simulation** model would be incorrect...illegal Verilog RTL **synthesis** coding style) the **simulation** model would not be correct for a **flip-flop** and Synopsys would...reading the model for **synthesis**. For VHDL, including...
more hits
from [http://web.engr.oregonstate.edu/~traylor/ece474/resets...]
similar results

2. DOT/FAA/AR-95/31 Design, Test, and Certification [Word-501K]
Apr 2005
...Describing the Design 52 4.4 **Synthesis** of Digital Logic 62 4.5...Verification and Validation 139 7.2 **Simulation** 141 7.3 Additional Considerations for **Simulation** 144 7.4 Application Specific...for Positive Edge Clocked **Flip-Flop** 34 v 22 Synchronization...Coding Example 61 32 Logic **Synthesis** Process 64 33a Hierarchical...
[http://www.faa.gov/certification/aircraft/av-info/soft...]
similar results

3. EE5319/EE4328 - Spring, 2002 Homework 2 Complete by 30 January 2002 [PPT-91K]
Nov 2004
...and then **simulation** B. **simulation**, then FPGA place & route, and then **synthesis** C. **simulation**, then **synthesis**, and then FPGA place & route...Signal C. Both of them 7) A D **flip-flop** output can become **metastable** when: A. the clock is too...
more hits from [http://www-ee.uta.edu/online/liu/ee5319_fall04/exam/EX...]
similar results

4. Ian G. Clark - Metastability Bibliography [94K]
Sep 2004
...Synchronizers Operating in **Metastable** Region", IEEE Transactions...Dynamics of Bistable **Flip**-Flops", 6th Int. Symp...Davies,

Did you mean?
Simulation synthes ("metastable flow"

Refine your sear using these key found in the res
- arbitration
- capacitance
- clock cycle
- clocked
- clock period
- design flow
- digital systems
- dual-rail
- hold time
- metastability
- phase detector
- phase error
- programmable
- setup time
- test bench
- truth table

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3	INZZ	2 AND simulation	unrestricted	1139	show titles
4	INZZ	3 AND synthesis	unrestricted	11	show titles

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Scholar Results **1** - **10** of about **135** for **simulation and synthesis and metastable and flip flop**. (**0.07** secor

Simulation and Synthesis Techniques for Asynchronous FIFO Design with Asynchronous Pointer ...
CE Cummings, P Alfke - SNUG 2002 (Synopsys Users Group Conference, San Jose, CA, ..., 2002 - sunburst-design.com
... **Simulation** and **Synthesis** Techniques for ... The first **flip-flop** could go **metastable**, which is why there is a second **flip-flop** in the dual synchronizer. ...
Cited by 3 - View as HTML - Web Search - sunburst-design.com - eda.ee.nctu.edu.tw

SAME 2004
S Bernardi, S Lebailly, T Instruments, B Blanc, G ... - signal - same-conference.org
... top-level is valid for **simulation** and verification ... reduction of compilation and **synthesis** time • Better ... or hold time; thus, causing a **metastable** condition and ...
View as HTML - Web Search - same-conference.com

Using hierarchical clock tree **synthesis** to generate balanced clock trees
P Ragon, A Dugar - Integr. Syst. Des, 1997 - eedesign.com
... cause **flip**-flops to operate in **metastable** states and ... However, because **simulation** requires developing test vectors, we ... The ASIC **synthesis** tool we had chosen had ...
Cited by 1 - Cached - Web Search - eedesign.com

Synchronous Resets? Asynchronous Resets? I am so confused! How will I ever know which to use?
CE Cummings, D Mills - SNUG 2002 (Synopsys Users Group Conference, San Jose, CA, ..., 2002 - sunburst-design.com
... add any **synthesis** attributes to get the **synthesis** tool to ... is not part of cycle based **simulation**, the asynchronous ... of the **flip-flop** could go **metastable** and thus ...
Cited by 3 - View as HTML - Web Search - bluegge.y365.com - all 8 versions »

Communication Between Independent On-Chip Synchronous Systems
I Brynjolfson - macs.ece.mcgill.ca
... N. Vijaykrishnan, "Energy Efficient Datapath **Synthesis** Using Dynamic ... and R. Brodersen, "The **Simulation** and Evaluation ... to obtain a **metastable** response from ...
View as HTML - Web Search

A METHOD FOR HIGH RELIABILITY FIELD PROGRAMMABLE GATE ARRAY (FPGA) DESIGNS
D Albaijes, FE Branch - klabs.org
... Does timing **simulation** meet functional and performance requirements? Return to DESIGN, **SYNTHESIS**, or PLACE & ... result in **metastable** conditions at the synchronizer ...
View as HTML - Web Search

Verifying Synchronization in Multi-Clock Domain SoC
T Kapschitz, R Ginosar, R Newton - 2004 - athdl.com
... timing violations may cause signals to go **metastable**; they also ... www.athdl.com/products.html [5] Cliff Cummings, "**Simulation** and **Synthesis** Techniques for ...
Cited by 1 - View as HTML - Web Search - cs.huji.ac.il

Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs
CE Cummings - Synopsys Users Group Conference, San Jose, CA, www. sunburst ..., 2001 - vlsidsp.el.yuntech.edu.tw
... detail some of the hardware design, timing analysis, **synthesis** and **simulation** methodologies to ... and might still be **metastable** at the next rising edge of ...
Cited by 3 - View as HTML - Web Search - eecg.toronto.edu - all 8 versions »

Asynchronous & Synchronous Reset Design Techniques-Part Deux
CE Cummings, D Mills, S Golson - SNUG Boston 2003 - sunburst-design.com
... add any **synthesis** attributes to get the **synthesis** tool to ... is not part of cycle based **simulation**, the asynchronous ... of the **flip-flop** could go **metastable** and thus ...
Cited by 2 - View as HTML - Web Search - trilobyte.com - klabs.org - lcdm-eng.com - all 5 versions »

High speed externally asynchronous/internally clocked systems
WS VanScheik, RF Tinder - IEEE Transactions on Computers, 1997 - ieeexplore.ieee.org
... manner similar to edge-triggered D **flip-flop**, but with ... Studies of the **metastable** condition rele- vant to this ... 7. DL-DFLOP NOR sequence recognition **simulation**. ...
Cited by 7 - Web Search - doi.ieeecs.org - doi.ieeecomputersociety.org - portal.acm.org - all 7 versions »

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simulation and synthesis and metastable filety Search Advanced Search Preferences

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Expert Verilog, SystemVerilog & **Synthesis** Training. **Simulation** and **Synthesis** ...
avoid **metastable** problems as described below). This is not a problem. ...
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some of the hardware design, timing analysis, **synthesis** and **simulation** ...
Synchronization failure is caused by an output going **metastable** and not ...
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[PDF] Design Elements
File Format: PDF/Adobe Acrobat - View as HTML
cific problem is to avoid **metastable** states which might drive the FSMs into unknown
... [1] Clifford E. Cummings, Peter Alfke, **Simulation** and **Synthesis** ...
mufasa.informatik.uni-mannheim.de/ Lectures/SS05/HWE/script/fifos.pdf - Similar pages

[PDF] USING ASSERTION-BASED VERIFICATION TO VERIFY CLOCK DOMAIN CROSSING ...
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designers to add synchronizers to reduce the probability of **metastable** signals
... automatically finds common RTL errors, **simulation**-to-**synthesis** mismatch ...
www.0-in.com/papers/dvcon2003.pdf - Similar pages

[PDF] Research Area 4 **Metastable** Alloys
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Crystallization" deal with the **synthesis**. of **metastable** amorphous and crystalli-
... Using **simulation** techniques the. structure of these materials could be ...
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[PDF] 4.3. Theory, **Simulation** and Design of Advanced Ceramics and Composites
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Unfortunately the influence of **metastable** phases, kinetic. effects and non-equilibrium
conditions, ... tion and improved **synthesis** methods provide greater ...
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[PDF] 9.1. Materials Phenomena and Techniques
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simulation of materials **synthesis**, processing, micro- ... **Metastable** and inhomogenous
materials. Modelling of Industrial Materials (large length-large time ...
www.mpg.de/pdf/europeanWhiteBook/ wb_materials_291_296.pdf - Similar pages

[PDF] MECHANICAL PROPERTIES RESEARCH LABORATORY (MPRL) 1995-1996 Annual ...
File Format: PDF/Adobe Acrobat - View as HTML
Development of improved constitutive models and **simulation** capability for processing !
... Title: "**Synthesis** of **Metastable** Carbon-Silicon Nitride by ...

www.me.gatech.edu/MPRL/MPRLRPT.96.PDF - Similar pages

[PDF] Asynchronous & Synchronous Reset Design Techniques - Part Deux
File Format: PDF/Adobe Acrobat - View as HTML
Example 6 – Verilog Asynchronous SET/RESET **simulation** and **synthesis** model ...
flip-flop could go **metastable** and thus the reset state of the ASIC could be ...
klabs.org/richcontent/General_ Application_Notes/reset_sync_async_v2.pdf - Similar pages

[PDF] ODELING AND IMULATION Table 102 Modeling and **Simulation** Difficult ...
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Resolution enhancement techniques; mask **synthesis** (OPC, PSM) ... Table 103a
Modeling and **Simulation** Technology Requirements: Capabilities—Near-term ...
public.itrs.net/Files/ 2002Update/2002Update-Modeling.pdf - Similar pages

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